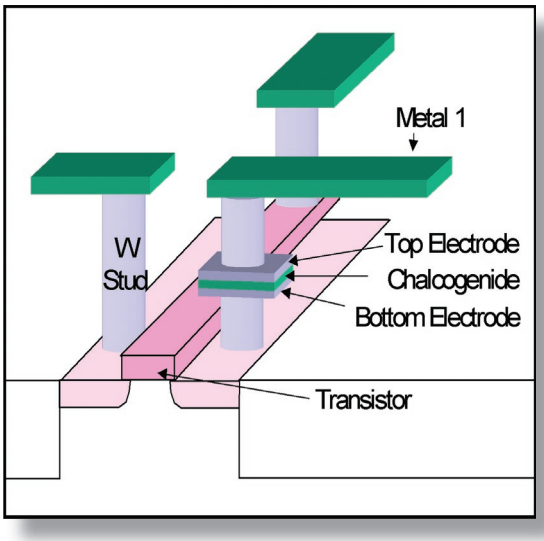
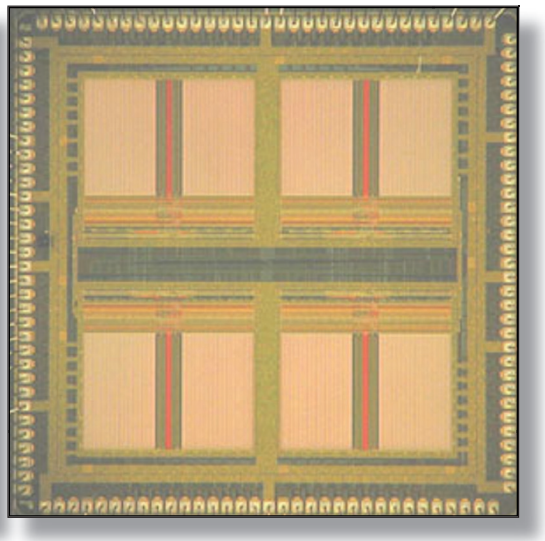
Air Force Research Laboratory|AFRL

Science and Technology for Tomorrow's Air and Space Force

Success Story

AFRL DEMONSTRATES NEW NON-VOLATILE MEMORY TECHNOLOGY





The Space Vehicles Directorate's Space Electronics and Protection Branch recently announced the "first-pass success" of a 64 kbit non-volatile memory array. This chalcogenide-based random access memory (C-RAM) is an electrically non-volatile, solid-state memory with significant advantages over other non-volatile memory types. Most military satellites are highly dependent upon non-volatile memory.

This C-RAM solution offers the only known manufacturable route to radiation-hardened, non-volatile memory well beyond the 1Mbit level. The higher densities have the advantage of reduced power and weight.

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Accomplishment

The directorate and its contractors, BAE SYSTEMS Ovonyx, designed, fabricated, and tested test chips to demonstrate full integration of a chalcogenide-based memory element into a radiation-hardened complementary metal oxide semiconductor (CMOS) process.

Electrical test results on the first packaged parts indicate full functionality of the 64 kbit memory arrays—unprecedented for such new and unique material integration. Test results also confirmed that the insertion of a chalcogenide manufacturing flow had no effect on measured CMOS transistor parametrics and did not change the total dose response of the base technology.

Background

While "chalcogenide" refers to any alloy containing a majority of a Group VI element (sulfur, selenium, and tellurium), the chalcogenide alloy in this application is a carefully crafted combination of germanium, antimony, and tellurium. This alloy can change between two room-temperature phases—a highly ordered polycrystalline phase and a disordered amorphous phase—by appropriate heating and cooling.

There are both optical and electrical differences between the phases. The polycrystalline phase has about 14% higher reflectance and 2-6 orders of magnitude greater electrical conductivity than the amorphous phase.

Manufacturers of the non-volatile memory chip use conventional semiconductor memory fabrication methods to deposit a tiny volume of chalcogenide material for each bit location. The phase of the chalcogenide is then changed by electrically heating and cooling the material at a controlled rate. The power required is a function of volume; directorate researchers demonstrated currents as low as 10µA at 5V per bit, making the memory as good or better than other memory technologies for low power applications.

The non-volatile memory chip senses the state of the bit (one or zero) from the very large resistance difference. Since the information is stored in the phase of the material at each bit location, no power is required to maintain the data on the chip. Also, the material itself is intrinsically highly resistant to radiation from natural space or nuclear environments, so that simply starting with a radiation-hardened semiconductor process may develop radiation-hard memory chips.

Space Vehicles
Emerging Technologies

Additional information

To receive more information about this or other activities in the Air Force Research Laboratory, contact TECH CONNECT, AFRL/XPTC, (800) 203-6451 and you will be directed to the appropriate laboratory expert. (03-VS-16)